VLSI
TECHNOLOGY
ADVANCED DIGITAL SYSTEM DESIGN

CURRICULUM

6 WEEKS

LEVEL-1

» Introduction to VLSI [5 Hrs]

- What is VLSI
- VLSI Design Flow
- ASIC
- Soc

LEVEL A:

» Fundamentals of Digital Design

FUNDAMENTSLS [5 Hrs]

- Basis Digital Circuits
- Logic gates & Boolen Algebra
- Number Systems
- Digital Logic Families

Combinational Logic Design [10 Hrs]

- Multiplexers
- MUX based design for digital circuits
- Demultiplexers/Decoders
- Adders/Sub tractors
- BCD Arithmetic & ALU
- Comperators & Parity Generator
- Code Converters/Encoders
- Decoders
- Multiplers/Divider

Sequential Logic Design Principles [10 Hrs]

- Bistable Elements.
- Latches and Flip-Flops
- Counters and its application
- Synchronous Design methodology
- Impediments to Synchronous Design
- Shift Registers
- Design Examples & Case studies

Section B:

» Advanced Digital Design [15 Hrs]

- Synchronous/Asynchronous Sequential Circuits.
- Clocked Synchronous State-Machine Analysis.
- Clocked Synchronous State-Machine Design
- Finite State Machine
- Mealy and Moore machines
- State reduction technique
- Sequence Detectors
- ASM Charts
- Synchronizer Failure and Metastability Estimation
- Clock Dividers
- Synchronizers & Arbiters
- FIFO & Pipelining
- PLD + CPLD

Section C:

» VHDL [Optional]

Total Hrs: 30+20: L+P [50 Hrs]

- **VHDL OVERVIEW AND CONCEPTS:** Types, object classes, design units, compilation elaboration.
- **BASIC LANGUAGE ELEMENTS:** Lexical elements, syntax, operators, types and subtypes (scalar , physical, real, composite (arrays, records),access files).
- **CONTROL STRUCTURES:** Control Structures and rules (if, case, loop).
- **DRIVERS:** Resolution function, drivers (definition, initialization, creation), ports
- **TIMING:** Signal attributes. "wait" statement, delta time, simulation engine, modeling with delta time delays, VIT AL tables, inertial / transport delay
- **ELEMENTS OF ENTITY/ARCHITECTURE**ntity, architecture, (process, concurrent signal assignment, component instantiation and port association rules, concurrent procedure, generate, concurrent assertion, block, guarded signal).
- **SUBPROGRAMS:** Rules and guidelines (unconstrained arrays. interface class, initialization, implicit signal attributes, drivers, signal characteristics in procedure calls, sides ef fects),overloading, functions (resolution function, operator overloading, function(resolution function, operator overloading), concurrent procedure.
- **PACKAGES:** Declaration., body , deferred Constant, "use" Clause, Signals, resolution function, subprograms, converting typed objects to strings, TEXTIO, printing objects, linear feedback shift register , random number generation compilation order
- **USER DEFINED ATTRIBUTES, SPECIFICATIONS, AND CONFIGURATIONS:** Attribute declarations, attributes specifications, configuration specification and binding, configuration declaration and binding, configuration of generate statements.

- **DESIGN FOR SYNTHESIS:** Constructs, register inference, combinational logic inference. state machine and design styles, arthimetic operations.
- **FUNCTION MODELS AND TESTBENCHES:** Test bench design methodology , BFM Modeling, Scenario generation schemes, waveform generator , client/server , text command file, binary command file.
- **MINOR PROJECT**
- **VITAL:** Overview, features, model, pin-to-pin delay modeling style, distributed delay modeling style.
- **LAB SESSIONS ON MODELSIM**

Section C:

» VERILOG [Optional]

Total Hrs: 30+20:L+P

- **Overview of Digital Design with V erilog ® HDL**
  Evolution of CAD, emergence of HDLs, typical HDL-based design flow , why Verilog HDL?, trends in HDLs.
- **Hierarchical Modeling Concepts**
  Top-down and bottom-up design methodology , differences between modules and module instances, parts of a simulation, design block, stimulus block.
- **Basic Concepts**
  Lexical conventions, data types, system tasks, compiler directives.
- **Modules and Ports**
  Module definition, port declaration, connecting ports, hierarchical name referencing.
- **Gate-Level Modeling**
  Modeling using basic V erilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-of f delays, min, max, and typical delays.
- **Dataflow Modeling**
  Continuous assignments, delay specification,expressions, operators, operands, operator types.
- **Behaviour Modeling**
  Structured procedures, initial and always, blocking and nonblocking statements, delay control, generate statement, event control, conditional statements, multiway branching, loops, sequential and parallel blocks.
- **Tasks and Functions**
  Differences between tasks and functions, declaration, invocation, automatic tasks and functions,
- **Useful Modeling T echniques**
  Procedural continuous assignments, overriding parameters, conditional compilation and execution, useful system tasks.

» LIVE PROJECTS

List of projects [35 Hrs]

- Microcontroller Design
- RISC & CISC Processor Design
- Multiplier / Divider using dif ferent Algorithms
- DDR Controller
- I2C,AMBA, Wishbone Conmax
- JTAG: Boundary SCAN
- JPC, PCI, Ethernet
- CORDIC Algorithm