# VLSI
## TECHNOLOGY
### SYSTEM VERILOG WITH TCL

## CURRICULUM

» **Six Week Industrial Training on Advanced  VLSI-Verification using SystemVerilog and basic scripting**

- Course Type - Hands-on Training
- Duration - 6 weeks(Including week-off)
- Eligibility- BE/BTech/ME/Mtech
- Prerequisite - Digital,Verilog and C
- Tool - Modelsim ,Questasim

» **Course content**

» **Verification concepts in VLSI**

- VLSI Design Flow
- The Verification Process
- The Verification Methodology
- Basic Testbench Functionality
- Directed Testing
- Methodology Basics
- Testbench Components
- Layered Testbench
- Building a Layered Testbench
- Simulation Environment Phases
- Verification Flow in VLSI
- Verification domains and tools
- What is bug?
- Bug tools introduction etc.

» **System Verilog Basics**

- Introduction to systemVerilog
- Systemverilog Advantages over verilog and VHDL
- Use of system verilog in Industries and for Design
- Why SV for Verification?
- Data Types
- Operators
- Keywords
- Arrays
- Queue
- New constructs in SV
- Tasks and Functions
- Experiments on each constructs on lab

## » System Verilog for verification

- Object oriented paradigm (OOPs) – class introduction & inheritance
- Task Functions and Void Functions
- Procedural statements and routines
- Creating new Objects
- Memory allocation
- Writing verification environment

## » Basic Scripting using Tcl

- Introduction
- Data types, variables, assignments and expressions
- Lists, arrays and associative arrays
- Subroutines or Procedures
- Control structures
- File Input and Output
- The world of regular expressions
- More on TCL - trace, eval, exec, info, history, format

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