VLSI
TECHNOLOGY
VHDL TRAINING

CURRICULUM

» Introduction to VLSI

- What is VLSI
- VLSI Design Flow
- ASIC
- SoC

SECTION A:
» Fundamentals of Digital Design
FUNDAMENTALS

- Basic Digital Circuits
- Logic gates & Boolean Algebra
- Number System
- Digital Logic Families

» Combinational Logic Design

- Multiplexers
- MUX based design for digital circuits
- Demultiplexers/Decoders
- Adders/Sub tractors
- BCD Arithmetic & ALU
- Comparators & Parity Generator
- Code Converters/Encoders
- Decoders
- Multipliers/Divider

» Sequential Logic Design Priciples

- Bistable Elements,
- Latches and Flip-Flops
- Counters and its application
- Synchronous Design Methodology
- Impediments to Synchronous Design
- Shift Registers
- Design Examples & Case studies

SECTION B:
» Advanced Digital Design

- Synchronous/Asynchronous Sequential Circuits
- ASM charts
- Finite state machine
- Mealy and Moore machine
- State reduction technique
- Sequence Detectors
- Clock Dividers
- Synchronizers & Arbiters
- FIFO & Pipelining

Section C:
» VHDL

- **VHDL OVERVIEW AND CONCEPTS:** Types, object classes, design units, compilation elaboration.
- **BASIC LANGUAGE ELEMENTS:** Lexical elements, syntax, operators, types and subtypes (scalar, physical, real, composite (arrays, records),access files).
- **CONTROL STRUCTURES:** Control Structures and rules (if, case, loop).
- **DRIVERS:** Resolution function, drivers (definition, initialization, creation), ports
- **TIMING:** Signal attributes. “wait” statement, delta time, simulation engine, modeling with delta time delays, VITAL tables, inertial / transport delay
- **ELEMENTS OF ENTITY/ARCHITECTURE:** Entity, architecture, (process, concurrent signal assignment, component instantiation and port association rules, concurrent procedure, generate, concurrent assertion, block, guarded signal).
- **SUBPROGRAMS:** Rules and guidelines (unconstrained arrays. interface class, initialization, implicit signal attributes, drivers, signal characteristics in procedure calls, sides effects),overloading, functions (resolution function, operator overloading, function(resolution function, operator overloading), concurrent procedure.
- **PACKAGES:** Declaration., body, deferred Constant, “use” Clause, Signals, resolution function, subprograms, converting typed objects to strings, TEXTIO, printing objects, linear feedback shift register, random number generation compilation order
- **USER DEFINED ATTRIBUTES, SPECIFICATIONS, AND CONFIGURATIONS:** Attribute declarations, attributes specifications, configuration specification and binding, configuration declaration and binding, configuration of generate statements.
- **DESIGN FOR SYNTHESIS**
  - Constructs, register interface,
  - combinational logic interface, state machine and
  - design styles, arithmetic operations.
- **FUNCTIONAL MODELS AND TESTBENCHES :**

- Test
- bench design methodology, BFM Modeling,scenario
- generation schemes, waveform generator, client/server,
- text command file, binary command file.

» **MINOR PROJECT**
Lab Sessions on ModelSIM

DUCAT®
development | consultancy | training

E-mail: info@ducatindia.com
Visit us: www.ducatindia.com
www.facebook.com/ducateducation

NOIDA
A-43 & A-52, Sector-16,
Noida - 201301, (U.P.) INDIA
70-70-90-50-90
+91 99-9999-3213

GHAZIABAD
1, Anand Industrial Estate,
Near ITS College, Mohan Nagar,
Ghaziabad (U.P.)
70-70-90-50-90

PITAMPURA (DELHI)
Plot No. 366, 2nd Floor,
Kohat Enclave, Pitampura,
(Near- Kohat Metro Station)
Above Allahabad Bank,
New Delhi- 110034.
70-70-90-50-90

SOUTH EXTENSION (DELHI)
D-27,South Extension-1
New Delhi-110049
70-70-90-50-90
+91 98-1161-2707

GURGAON
1808/2, 2nd floor old DLF,
Near Honda Showroom,
Sec.-14, Gurgaon (Haryana)
70-70-90-50-90